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EXAMINER

COLEMAN, ERIC

ART UNIT PAPER NUMBER

2183

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/777,934	Applicant(s) DEVANEY ET AL.	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1,2,8,9,11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
3. Claim 1 (lines 1,10,) , claim 11, (line 2)contains the “disposed on a peripheral region” and Claim 1 (line 10), claim 11.(line has “disposed at a central region” claim 11,(lines 3, and 7) contains disposed at a different quadrant claims 2(line 2)contains “disposed in the central region, Claim 2, (line 4),claim 11 (line 9) contains “disposed above”.
4. As to the “disposed of...” language, it is unclear the scope of the location of the elements of the claims (i.e., how close to the edge or center, or is the element directly above or above to the side or something else) further it is unclear whether the dispose language provided for any structural provision that would limit the changing the location of the element and does the disposing of the element provide any connection or coupling of elements where signals could be exchanged.
5. Claim 8 (line 5) contains size is a variable size predetermined by the compiler.
6. As to this if the size is predetermined is the size variable after it is predetermined or something else (i.e., can the size change after it is predetermined)?

7. Claim 9 comprises the limitation "free-of and automatic data cache" the scope of meaning of the this terminology is unclear (i.e., if the system comprises a cache how is it free of a cache and in what way it the cache not automatic.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-3,5,8,9,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keckler (patent No. 5,574,939) in view of Anderson (patent No. 6,594,711)(As per claims 1,5,8,9).

10. Keckler taught the invention substantially as claimed including a data processing ("DP") system comprising: A chip Multiprocessor (Map chip, e.g., see fig. 2, and col. 4, lines 28-42) comprising: plurality of processors disposed on the peripheral region of the chip (e.g., see figs.2, 3) each processor including a data path for executing instructions (e.g., see fig. 4 data path input to the pipeline and data path for results); compiler controller register file (50) coupled to the dual data path for holding operands (e.g., see col. 9, lines 48-56) of an instruction (e.g., see fig. 4)(compiler driven because the processors are VLIW processors e.g., see col. 1, lines 32-52 and col. 3, lines 41-57);compiler controlled local memory (70), a portion of the local memory for holding operands of an instruction (e.g., see fig. 4)Shared main memory (3) disposed on the

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chip (e.g., see fig. 3); crossbar switching system (e.g., see col. 5, lines 12-30) coupling the shared main memory to each of the plurality of processors (e.g., see fig. 3 and col. 6, lines 22-67) first-in-first-out system (78) for transferring operands of an instruction among multiple processors of the plurality of processors (e.g., see col. 9, lines 57-66).

11. Keckler did not expressly detail the data path was a dual data path, and the local memory with a portion disposed to the right of the dual data path and a portion disposed to the left of the dual data path. Anderson however taught a system with CPUs each comprising a dual data path (e.g., see fig. 6) with local memory (88) (e.g., see fig. 6) As to the disposing of portions of the local memory, Anderson taught a local memory that is partitioned (e.g., see col. 8, lines 25-39). Although the Keckler and Anderson portions of local memory are not detailed as disposed to the right or left, the operation of the system requires that the portions of the local memory be separate for the each data path (for data coherency each data path must have its own locations) and Anderson taught that the partitioning was in a conventional manner (e.g., see col. 8, lines 25-39). Therefore the operation of the local memory of Anderson and Keckler would have been the same as the claimed local memory even if the claimed local memory was separated physically and placed at different physical locations to the left and right (for the local memory portions to be portions of the same memory the memory portions would have had to be connected to each other and to the data paths that access them). Here both the claimed local memory portions and the Anderson and Keckler local memory comprise this feature. The equivalence of the use of one larger memory or plural smaller memories for the larger memory was well known in the art at the time of the

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claimed invention. One of ordinary skill in the art would have been motivated to replace the larger local memory by plural smaller memories depending on the cost of the larger memory versus the use of smaller memories and the space limitations of placing the memories on the chip. Anderson discussed that the decisions on the type and number of elements to place on a chip depends on the complexity of the circuit to be placed on the integrated circuit (e.g., see col. 5, lines 1-54).

12. As per claim 2,10 Keckler taught the shared main memory (e.g., see col. 6, lines 22-32). Keckler did not specify the type of memory. However the use of DRAM or SRAM was have been well known to be the types of memory available to use for memories. As to the use of DRAM over SRAM clearly one of ordinary skill would have used DRAM at least to reduce cost of memory. As to the location of the main memory and the crossbar and DRAM clearly this disposition is merely an arrangement of elements without change in operation and therefore does not provide any patentable distinction over the teachings Keckler. Further one of ordinary skill considering the plurality of processors requiring access to memory would have been motivated to allow overlapping read and write to the memory. This would have required a multiple buffers to allow the concurrent access. One of ordinary skill would have been motivated to implement the double buffering with a sense amplifier at least to allow the system to detect the condition when the concurrent access was needed.

13. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Anderson and Keckler. Both references were directed toward the problems of memory access in systems with plural processors (e.g., see col. 1, lines 11-51 of

Anderson and col. 5, lines 12-55 of Keckler). Therefore one of ordinary skill would have been motivated to incorporate the Anderson teachings of placing each of the processor in a clustered multiprocessor in a single chip at least to reduce size of the system and cost. (e.g., see col. 5, lines 1-25).

14. As per claim 3, Keckler taught each processor including at least one data port for accessing the shared main memory (e.g., see fig. 3 and col. 7, lines 30-63); As to the shared main memory including pages of embedded DRAM this was discussed above with respect to claim 2, and considering the teachings discussed above the one of ordinary skill would be motivated to use DRAM for the memory. The division of a DRAM in to pages was well known in the art at the time of the claimed invention.

15. Claims 4,6,7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keckler (patent No. 5,574,939) in view of Anderson (patent No. 6,594,711 as applied to claim 1-3,5 above, and further in view of Deneroff (patent No. 6,751,698).

16. As per claim 4, Deneroff taught a crossbar switch (810) coupling processor and memories (e.g., see fig. 8). Further use of split transaction bus in a crosspoint switch was well known in the art and one of ordinary skill would have been motivated to implement the cross point switch of Deneroff as split transaction to reduce cost and complexity that would be required of a cross point switch that comprise bidirectional busses.

17. As to claim 6,7, Deneroff taught a FIFO system that is configured to couple processors in a cluster of processor for transferring operands of an instruction between processors in the cluster (e.g., see fig. 8).

18. It would have been obvious to one of ordinary skill to combine the teachings Keckler and Deneroff. Both references were directed toward the problems of memory access in systems with plural processors (e.g., see col. 5, lines 12-55 of Keckler and col. 3, lines 33-46 of Deneroff). One of ordinary skill would have been motivated to incorporate the Deneroff teachings of FIFO memories at least to allow the processor to asynchronously transfer data between processors and memory.

19. Claims 11-14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (patent No. 6,594,711) in view of Dowling (patent application publication 2002/0091916 A1).

20. Anderson taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) first (411), second(412) third (413)and fourth(414) clusters of processors on a peripheral region of a chip each of the clusters of processors disposed at a different quadrant of the peripheral region of the chip(e.g., see figs. 2,4,5, and col. 6, lines 49-59 and col. 5, lines 1-37) each including a plurality of processors(78,80,82,84) for executing instructions (e.g., see fig. 6 and col. 8, lines 1-57); and

b) Memory access means (430,420) disposed in the central portion of the chip (e.g., see fig.4) .

21. Anderson did not expressly detail (claim 11) clusters of embedded DRAM. Dowling however taught Dram arrays comprising sixteen to sixty-four embedded DRAMs [that at least comprise first, second third, fourth etc. clusters] (e.g., see paragraph 0047 on page 8 and fig. 1); and mask and switching logic wherein one embodiment the switching logic comprises a full bit level crossbar switch (e.g., see paragraph 0058 on page 10). Therefore a full bit crossbar to handle at least sixteen DRAM arrays would have comprised at least 16 bits (i.e., at least one cross bar for each bit or each array). As to the disposition above the clusters, as the claim is understood, the operation of the system is the same whether the crossbar is elevated or on the same level as the other elements so the system of Anderson and Dowling that would comprise a crossbar switch comprising plural crossbars would have operated the same as the claimed invention.

22. As to the memory load/store instruction being executed by at least one processor in the clusters of processors by accessing at least one of the first second, third or fourth clusters of embedded DRAM by way of at least one of the first second and third and fourth crossbars. Dowling taught a load/store unit (e.g., see fig. 2 and paragraph 0057 on page 10). Clearly since the Dowling system was a programmed system the it would have been obvious to one of ordinary skill in the art that in at least one implementation of the Dowling teachings the load/store unit (226) would have performed load and store operation in response to a load/store instruction.

23. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Anderson and Dowling. Both references were directed toward the problems

of memory access in systems with plural processors (e.g., see col. 1, lines (11-51 of Anderson and col. paragraphs 002-005 on page 1 of Dowling). One of ordinary skill would have been motivated to incorporate the Dowling teachings of plural DRAM and the access to memory is via a crossbar switch at least to reduce the amount of area used on the chip reduce the delay in memory access (e.g., see paragraph 0010 on page 2 of Dowling).

24. As per claim 12, Anderson taught each of the plurality of clusters including a plurality of ports (input to the exemplary cluster 36a from TR Bus and data transfer bus 255 in figure 5 and ports 6a, 6b in figure 7) for accessing memory (e.g., see fig.7). As the access of embedded DRAM Dowling taught memory accessed by plurality processor comprised DRAM (e.g., see fig. 1)

25. As per claim 13, it was well known for crossbar switches to comprise horizontal and vertical busses coupled to the elements being switched with the connected made between the elements connected to the vertical line to the elements connected to the horizontal lines. Also taught Dowling taught the crossbar switch coupled to plural functional units and DRAM (e.g., see fig. 1). Therefore it would have been obvious to one of ordinary skill that in at least one implementation of the Anderson and Dowling teachings the horizontal busses of the crossbar switch would have been coupled to pages of the embedded DRAM while the vertical busses would have been connected to the processors (128).

26. As to claim 14, as understood the arbiters comprise means to determine which connections will be made within the crossbar switch for coupling elements connected to

the ports of the crossbar switch. Inherently a crossbar switch that can alter the connections between input and output as characteristic of conventional crossbar switches would have necessarily have comprised means to arbitrate or determine which connection is to be made (such determining which horizontal bus is to be coupled and which vertical bus is to be connected) (depending on some control signal(s)). Inputs for controlling signals are shown in figure 2 to crossbar unit (108) of Dowling or the mask control input 414 in figure 4 of Dowling.

27. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (patent No. 6,594,711) in view of Dowling (patent application publication 2002/0091916 A1) as applied to claims 11-14 above, and further in view of Deneroff (patent No. 6,751,698).

28. As to claim 15, Deneroff taught a FIFO system that is configured to couple processors in a cluster of processor for transferring operands of an instruction between processors in the cluster (e.g., see fig. 8).

29. As to claim 16, Deneroff taught the FIFO system includes a plurality of input FIFOs (e.g., see col. 12, line 52-col. 13, line 10) and a single output FIFO (e.g., see col. 11, line 65-col. 12, line 49) assigned to a processor in the cluster (e.g., see fig. 8).

30. It would have been obvious to one of ordinary skill to combine the teachings Anderson and Deneroff. Both references were directed toward the problems of memory access in systems with plural processors (e.g., see col. 1, lines 11-51 of Anderson and col. 3, lines 33-46 of Deneroff). One of ordinary skill would have been motivated to

incorporate the Deneroff teachings of FIFO memories at least to allow the processor to asynchronously transfer data between processors and memory.

31. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (patent No. 6,594,711) in view of Dowling (patent application publication 2002/0091916 A1) as applied to claims 11-14 above, and further in view of Keckler (patent No. 5,574,939).

32. As per claim 17, Keckler taught A chip Multiprocessor (Map chip, e.g., see fig. 2, and col. 4, lines 28-42) comprising: plurality of processors disposed on the peripheral region of the chip (e.g., see figs. 2, 3) each processor including a compiler controlled local memory (70), a portion of the local memory for holding operands of an instruction (e.g., see fig. 4)

33. As per claims 18,19 Keckler taught each processor including at least one data port for accessing the shared main memory (e.g., see fig. 3 and col. 7, lines 30-63); As to the shared main memory including pages of embedded DRAM as discussed above with respect to claim 2 the one of ordinary skill would be motivated to use DRAM for the memory. The division of a DRAM in to pages was well known in the art at the time of the claimed invention.

34. As per claim 20, Keckler taught the system comprised the capability of processing multiple threads across plural functional units (e.g., see col. 3, lines 41-56). Where eight threads can be processed for each of a plurality of nodes (e.g., see col. 4, lines 22-30). Therefore it would have been obvious to one of ordinary skill that the

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multithreading configuration provided for a configuration that was capable of receiving streaming media data.


35. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Anderson and Keckler. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Anderson and Keckler. Both references were directed toward the problems of memory access in systems with plural processors (e.g., see col. 1, lines (11-51 of Anderson and col. 5, lines 12-55 of Keckler). Therefore one of ordinary skill would have been motivated to incorporate the Keckler teachings of clustering of processors for processing plural threads in parallel at least to allow the combined system efficiently process data in streaming data applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



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PRIMARY EXAMINER